



```
    }
if {$make_assignments} {
  load_package project
  load_package flow
  set_global_assignment -name FAMILY "Cyclone II"
  set_global_assignment -name DEVICE EP2C35F672C6
  switch -exact -- $opt_strategy {
    1 {set_global_assignment -name CYCLONEII_OPTIMIZATION_TECHNIQUE AREA}
    2 {set_global_assignment -name CYCLONEII_OPTIMIZATION_TECHNIQUE SPEED}
    default
      {set_global_assignment -name CYCLONEII_OPTIMIZATION_TECHNIQUE BALANCED}
  }
  set_global_assignment -name DEVICE_FILTER_PACKAGE FBGA
  set_global_assignment -name DEVICE_FILTER_PIN_COUNT 672
  set_global_assignment -name DEVICE_FILTER_SPEED_GRADE 6
  set_global_assignment -name MIN_CORE_JUNCTION_TEMP 0
  set_global_assignment -name MAX_CORE_JUNCTION_TEMP 85
  set_global_assignment -name FMAX_REQUIREMENT $clock_freq
  foreach filename [glob $project_location/*.vhd] {
    set_global_assignment -name VHDL_FILE $filename
  }
}
if { $flow_mode=="short" } {
  execute_module -tool map
} else {
  # set_location_assignment -to port_name Pin_name
  execute_flow -compile
  set sof [pwd]/$project_name.sof
}
post_message -type info "Project $project_name is done"
```