

## Homework 4: NVRAM Interface

### Introduction

The NVRAM (Non-Volatile RAM) interface used to provide the access to the external serial NVRAM device through the parallel interface.

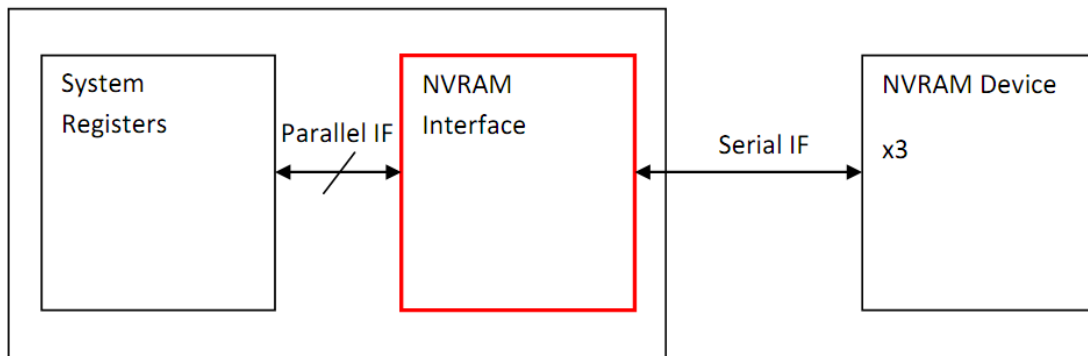


Figure 1: General Block Diagram

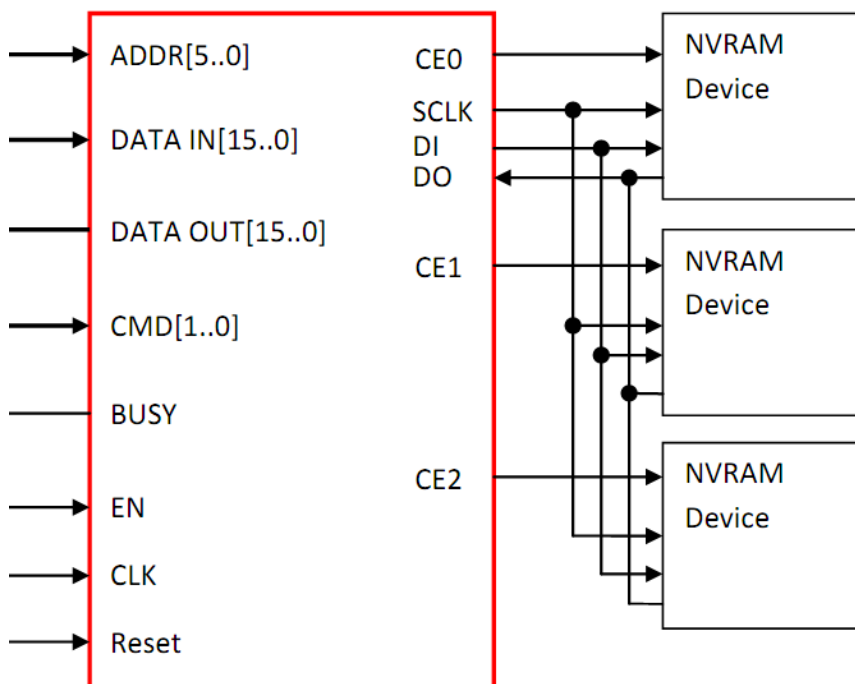


Figure 2: Detailed Block Diagram

## Port Definition

Port Name	IO	Description
ADDR[5..0]	Input	Specifies the address of the RAM. Used with READ and WRITE commands
DATA IN[15..0]	Input	Specifies the data that should be written to the memory. Used with WRITE command only.
DATA OUT[15..0]	Output	Specifies the data that should be received from the memory. Used with READ command only.
CMD[1..0]	Input	Specifies the command that should be issued to the memory: 00: READ 01: WRITE 10: ENABLE 11: Reserved
BUSY	Output	Indicates the interface status: 0: Idle 1: Busy
EN	Input	Specifies the start of command processing. The start command issued on the rising edge of the EN pulse.
CLK	Input	System Clock 62.5MHz
Reset	Input	System reset. Active High
CE0/1/2	Output	Chip Enable of the NVRAM Device. CE decoded according to the specified address: 0x00-0x0f: CE0 Active 0x10-0x1f: CE1 Active 0x20-0x2f: CE2 Active
SCLK	Output	Serial clock to the memory device. Should not exceed 1MHz
DI	Output	Serial data to the device
DO	Input	Serial data from the device

### The task:

1. For a detailed description of the principles of the NVRAM functioning use: <http://www.abramovbenjamin.net/malas/NVRAM.pdf>
2. Split the system (NVRAM\_IF) into two sub-system: OU and CU
3. Build a detailed block diagram of the OU (in primitives level, including the exact size of all components) and define the status and control signals
4. Build a state machine (state diagram only) for the CU