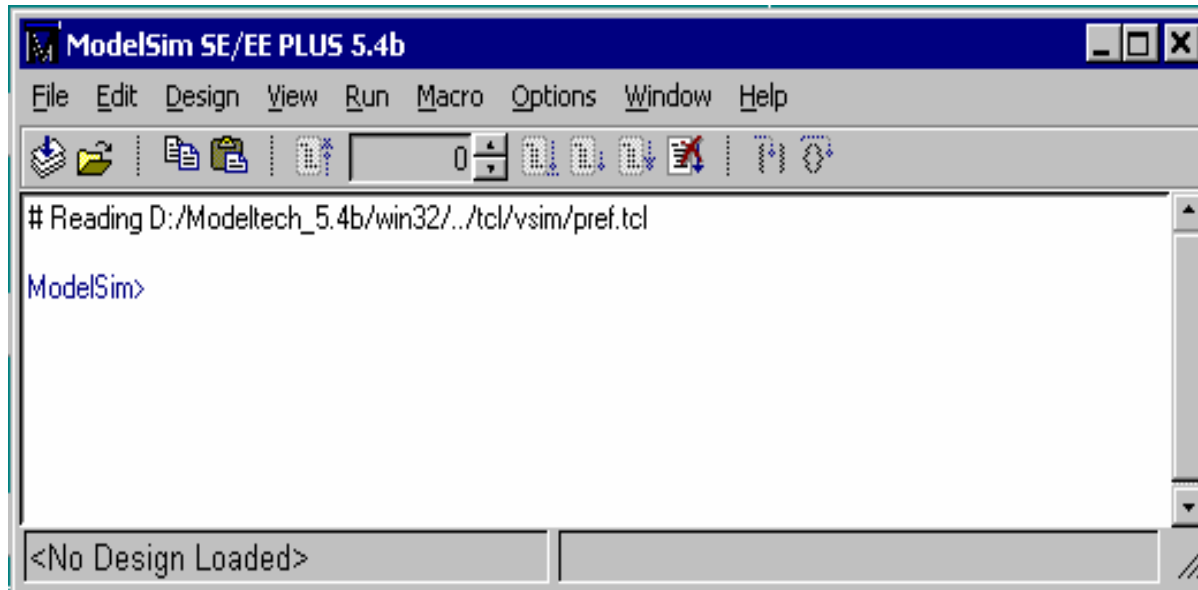


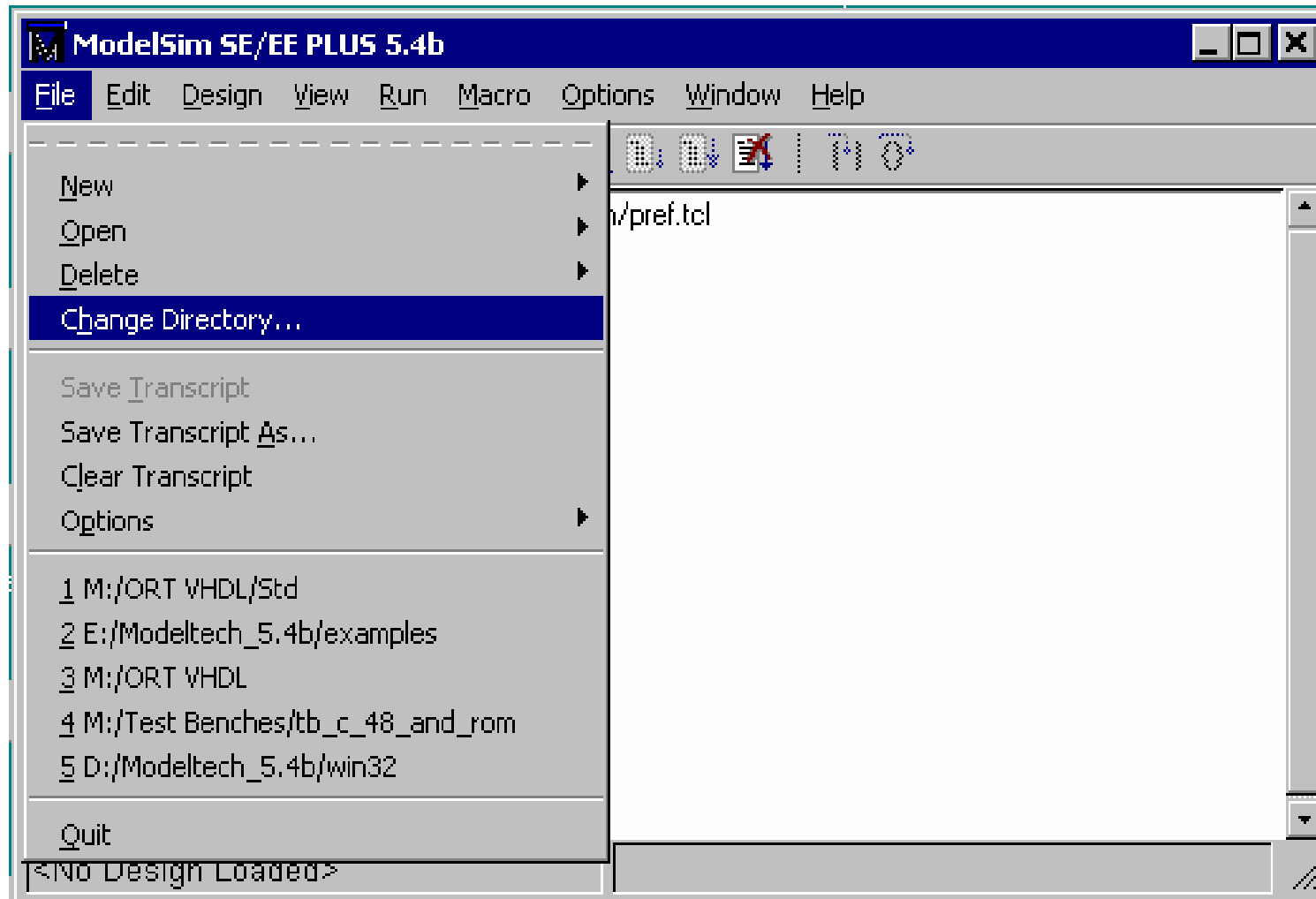
How to perform a simulation in **ModelSim**

- **Modelsim** is a simulation tool. It doesn't create any hardware, even on the monitor (as **Quartus** does). **Modelsim** just compiles the code, checks syntax and provides the waveform of the design behavior according to the inputs values defined at the **Test Bench** file. Therefore, **Modelsim** is a tool for the functional checking of the design.

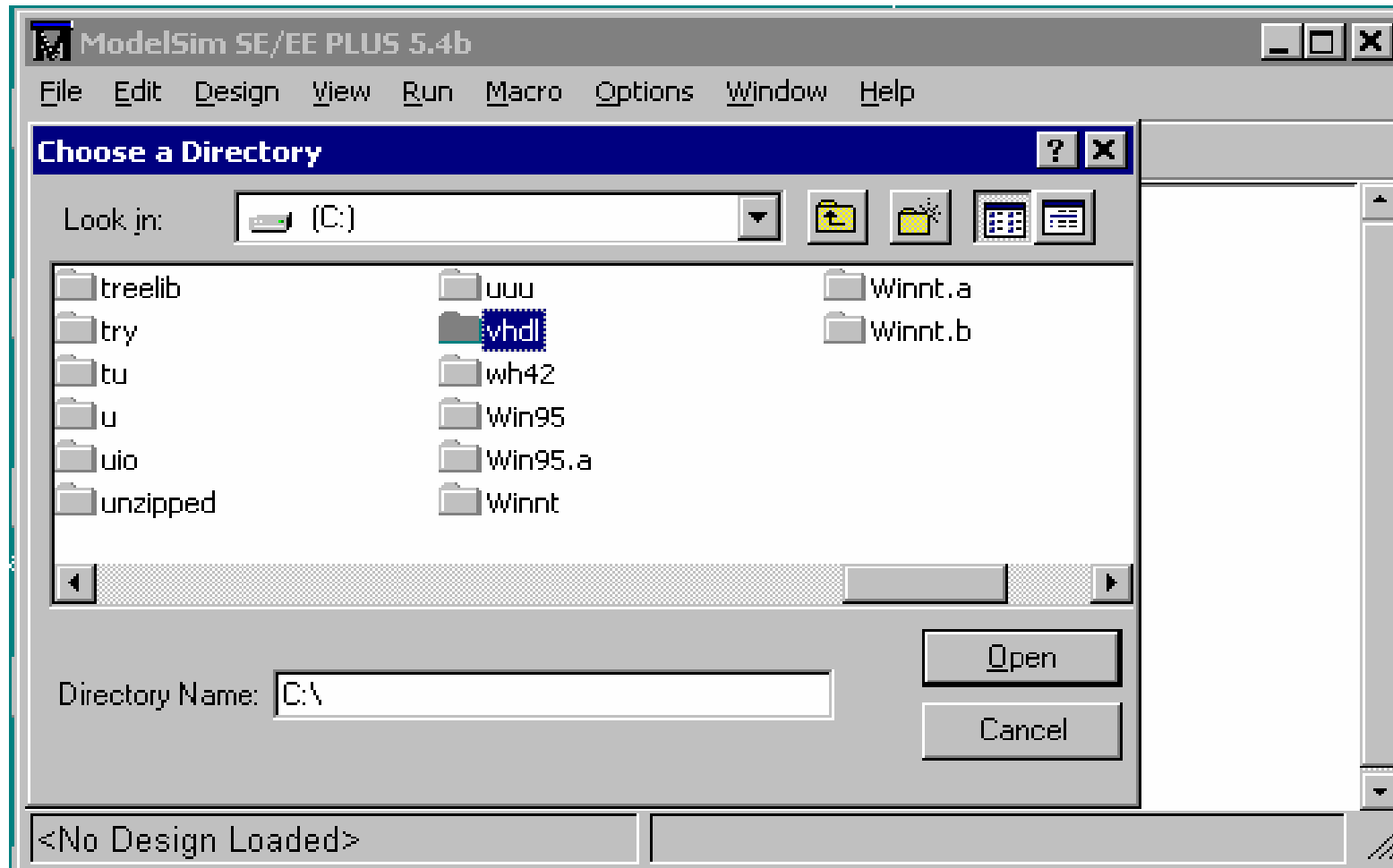
- Before starting to use **Modelsim**, be sure to have the design and its Test Bench codes saved at the C:\my_project library.
- The first step of using the program is to click the MODELSIM icon on the desktop or to enter from the Program Menu.



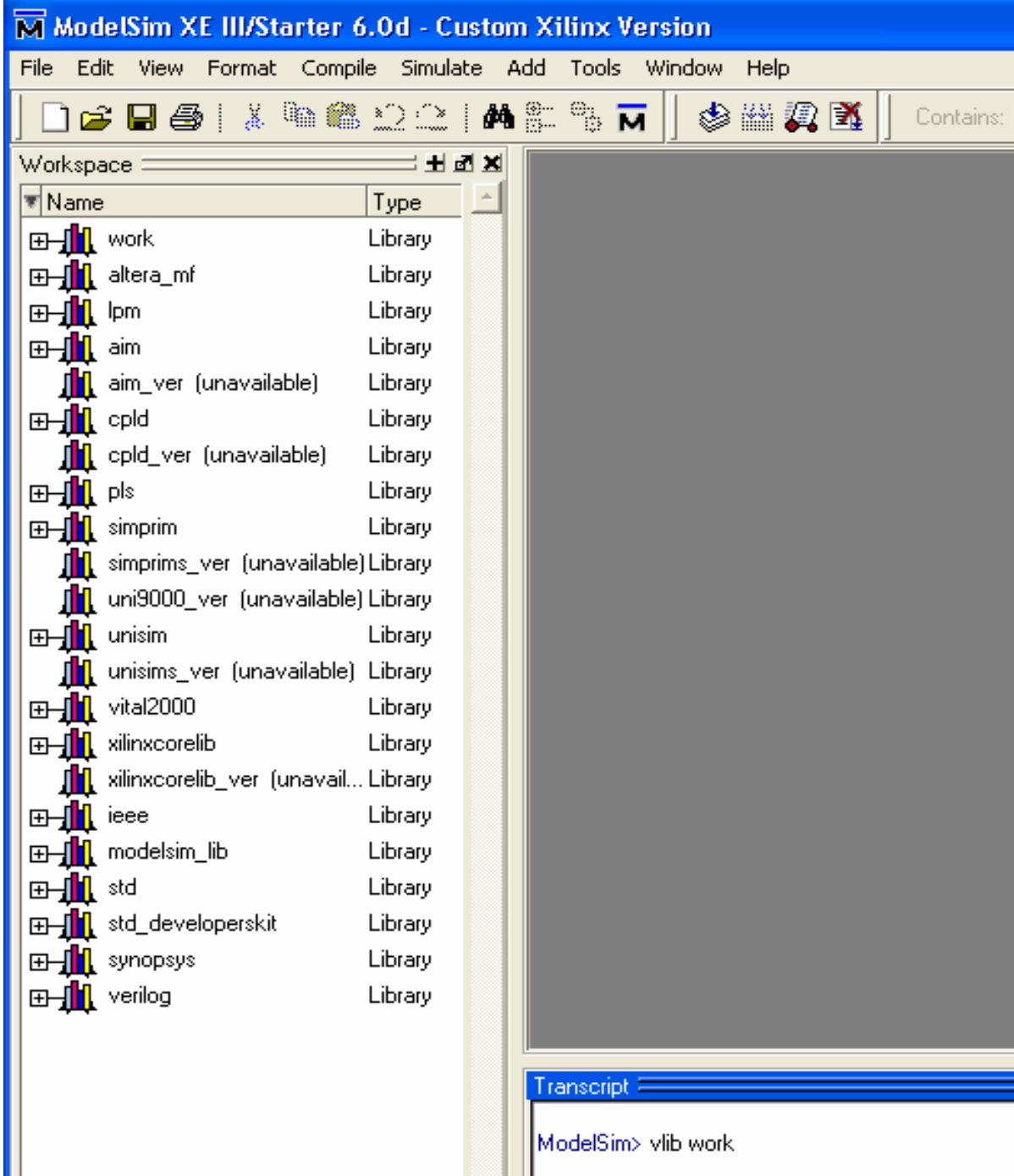
- Click File \ Change Directory...

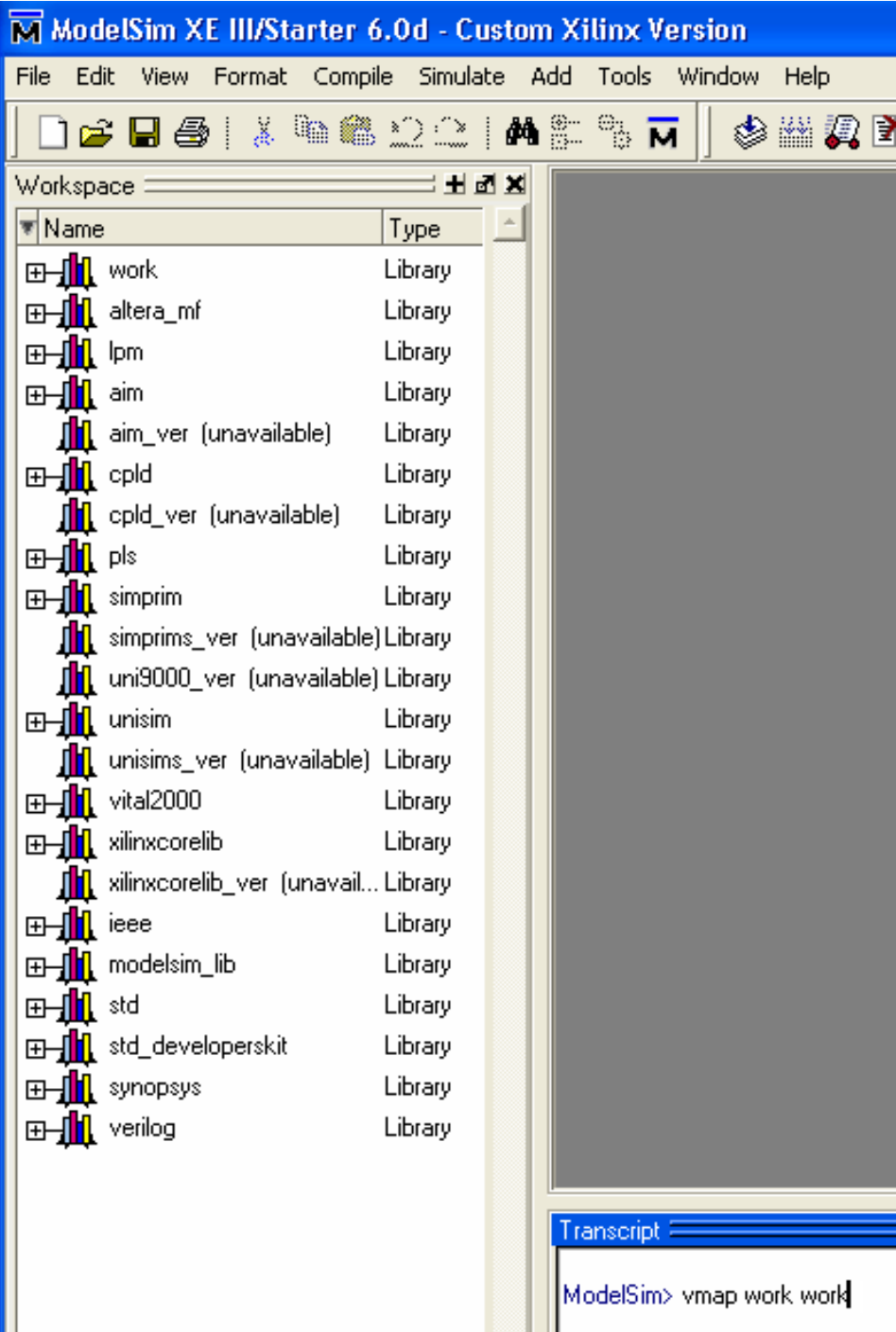


- Mark the desired directory and click OPEN...

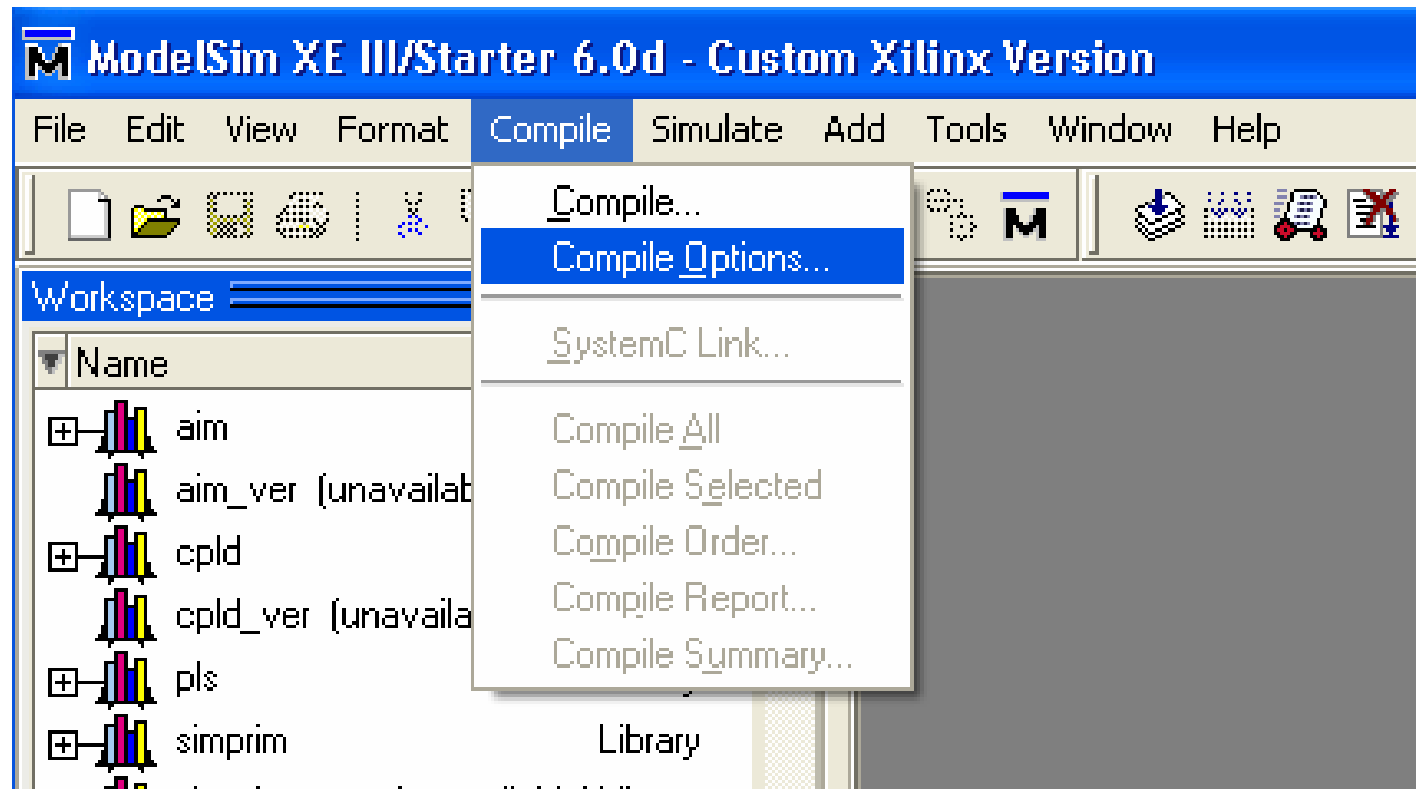


- Now you have to create a new directory by typing “vlib work “ command in transcript window for holding all compiled VHDL codes...
- Map the created physical folder work to virtual folder work by vmap command

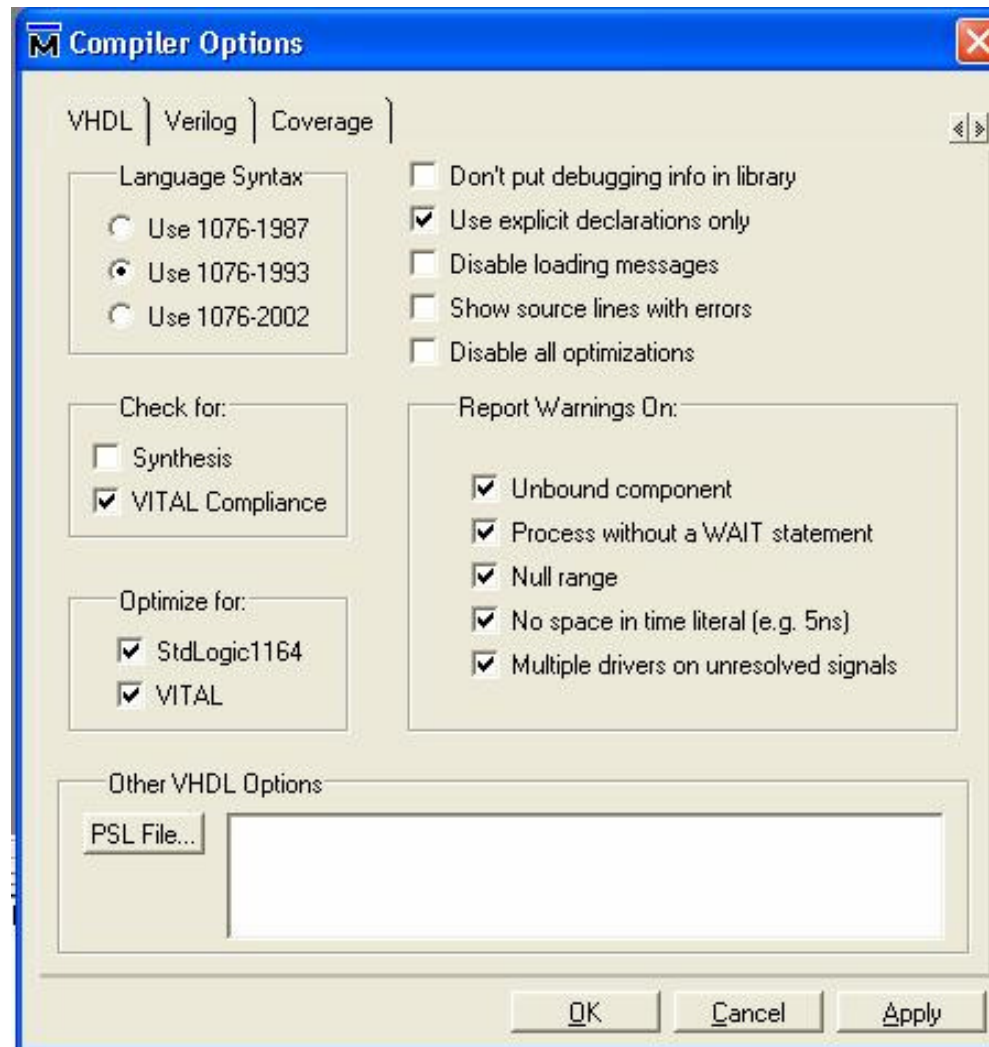




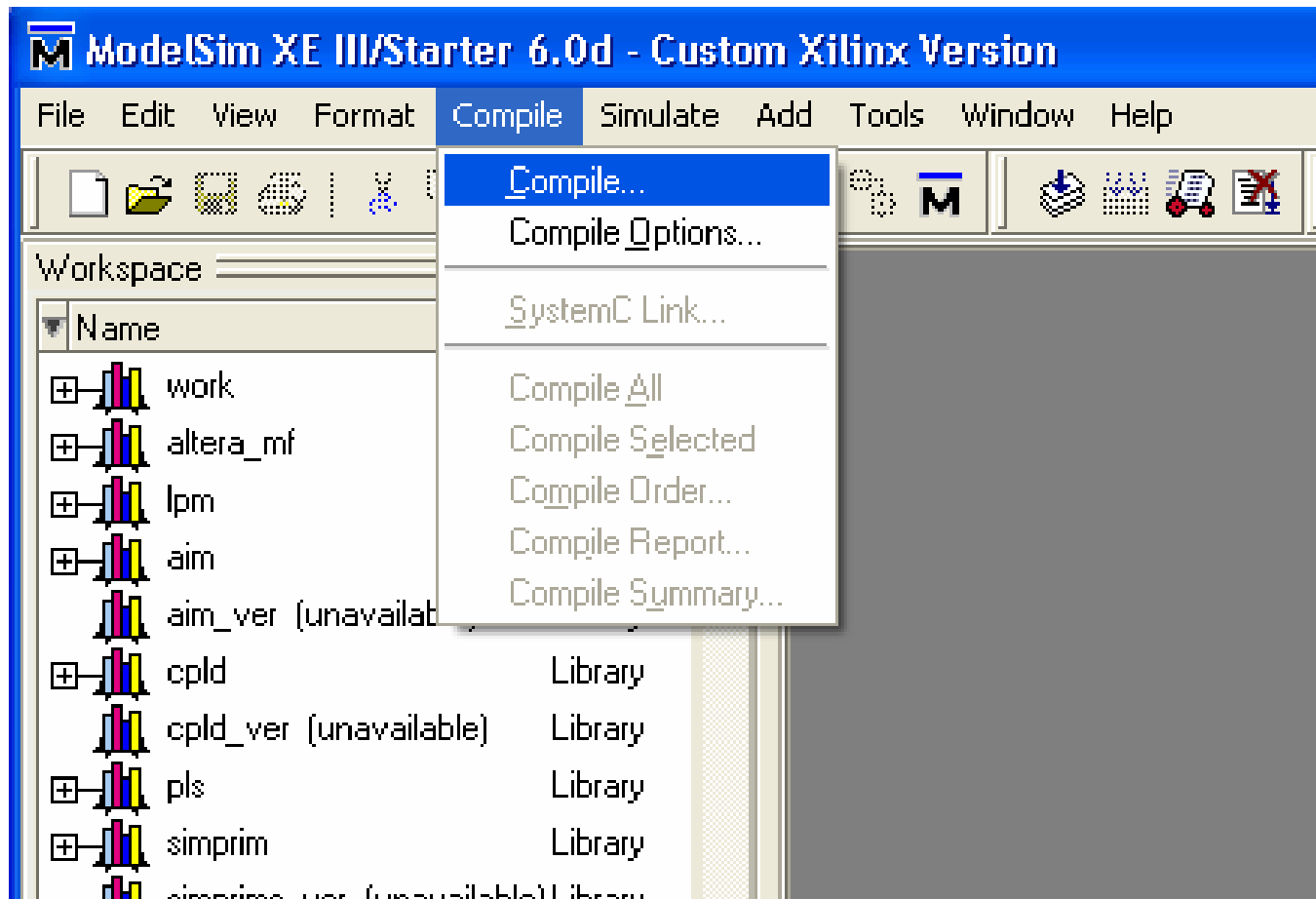
- Choose Compile\Options...



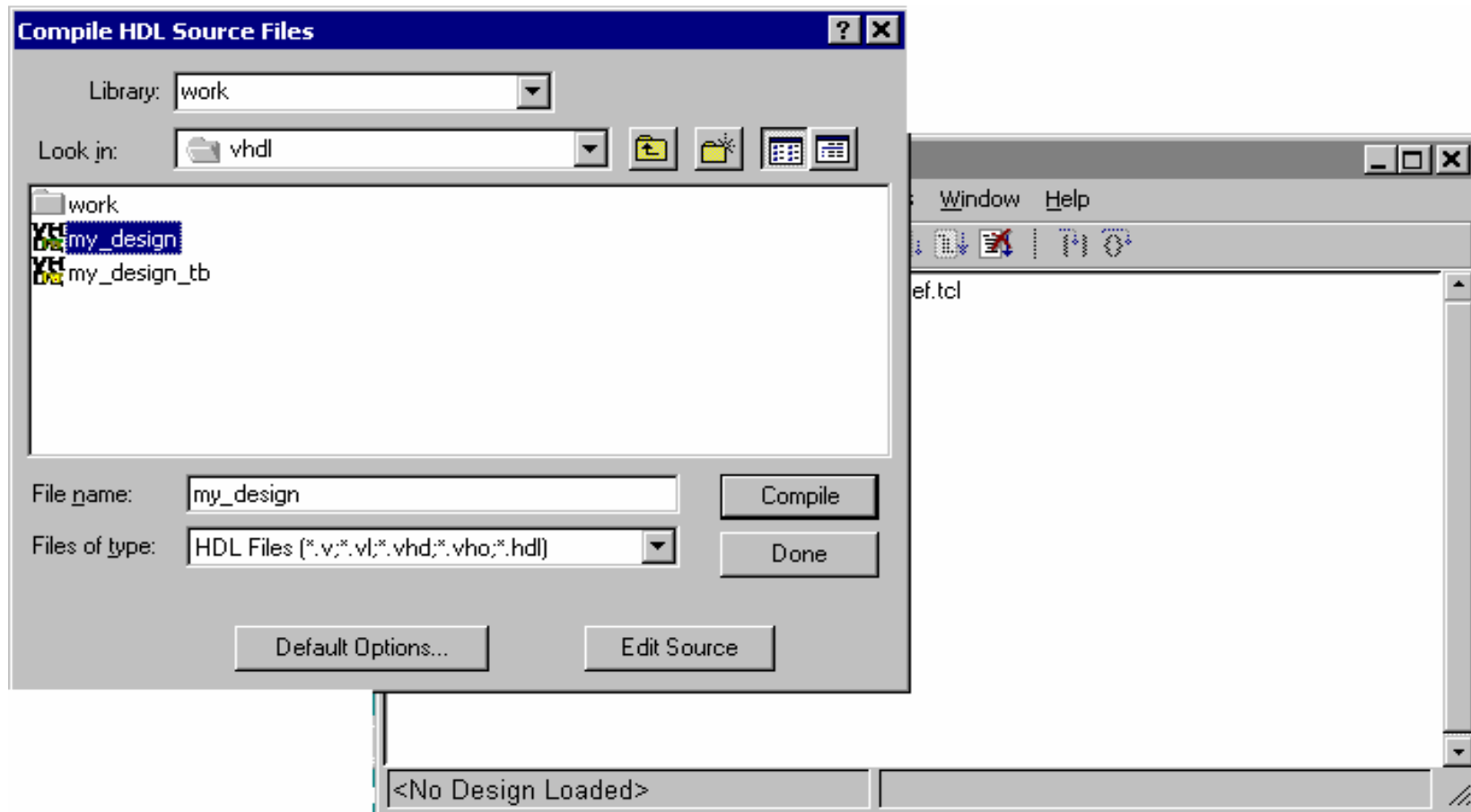
- Make sure that “Use 1993 Language Syntax” option is chosen...



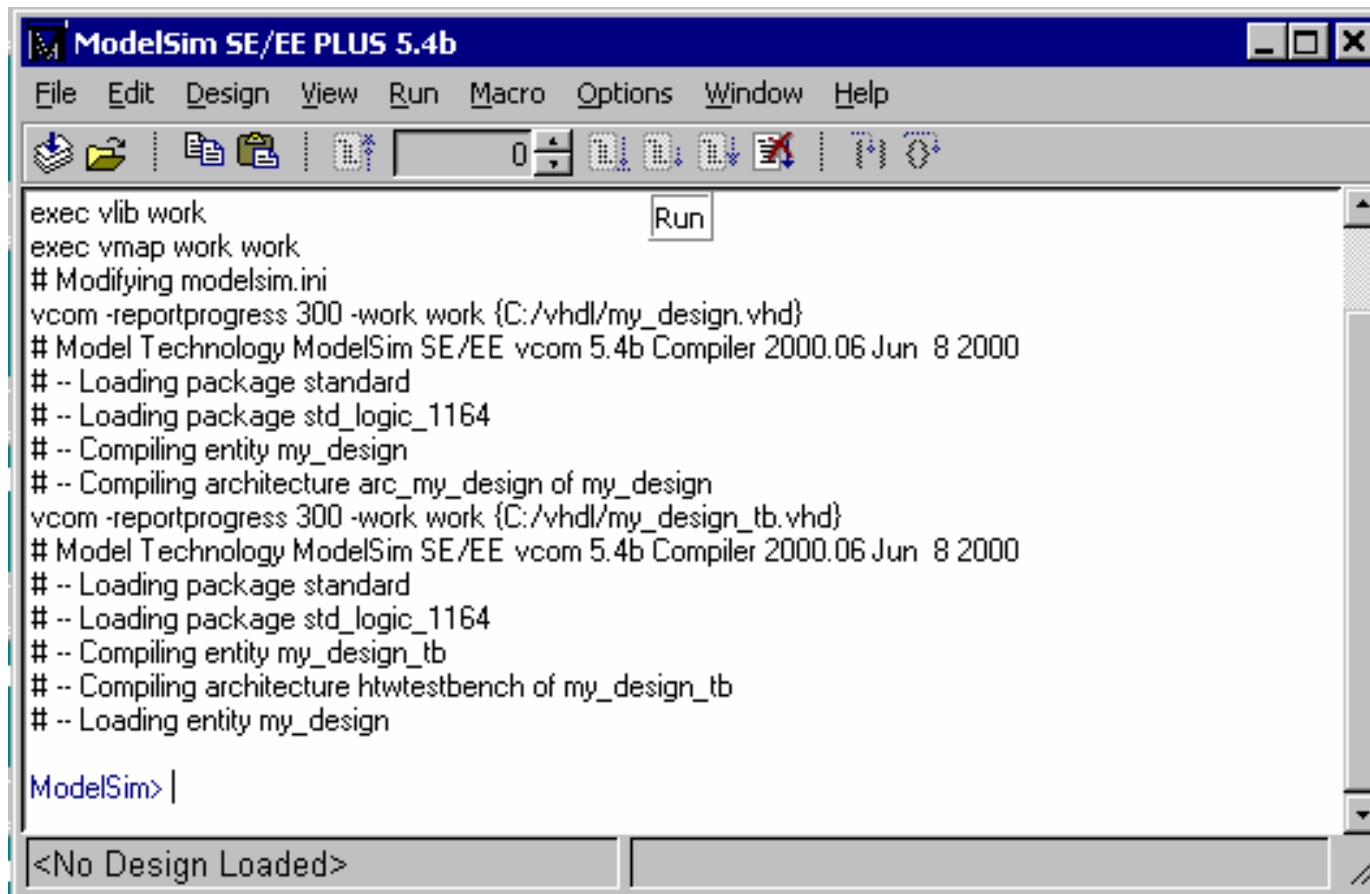
- Choose Compile\ Compile...



Compile your codes in the following order:
start from the lowest hierarchical level up to the
highest one. Afterwards compile the test bench
of the top level...



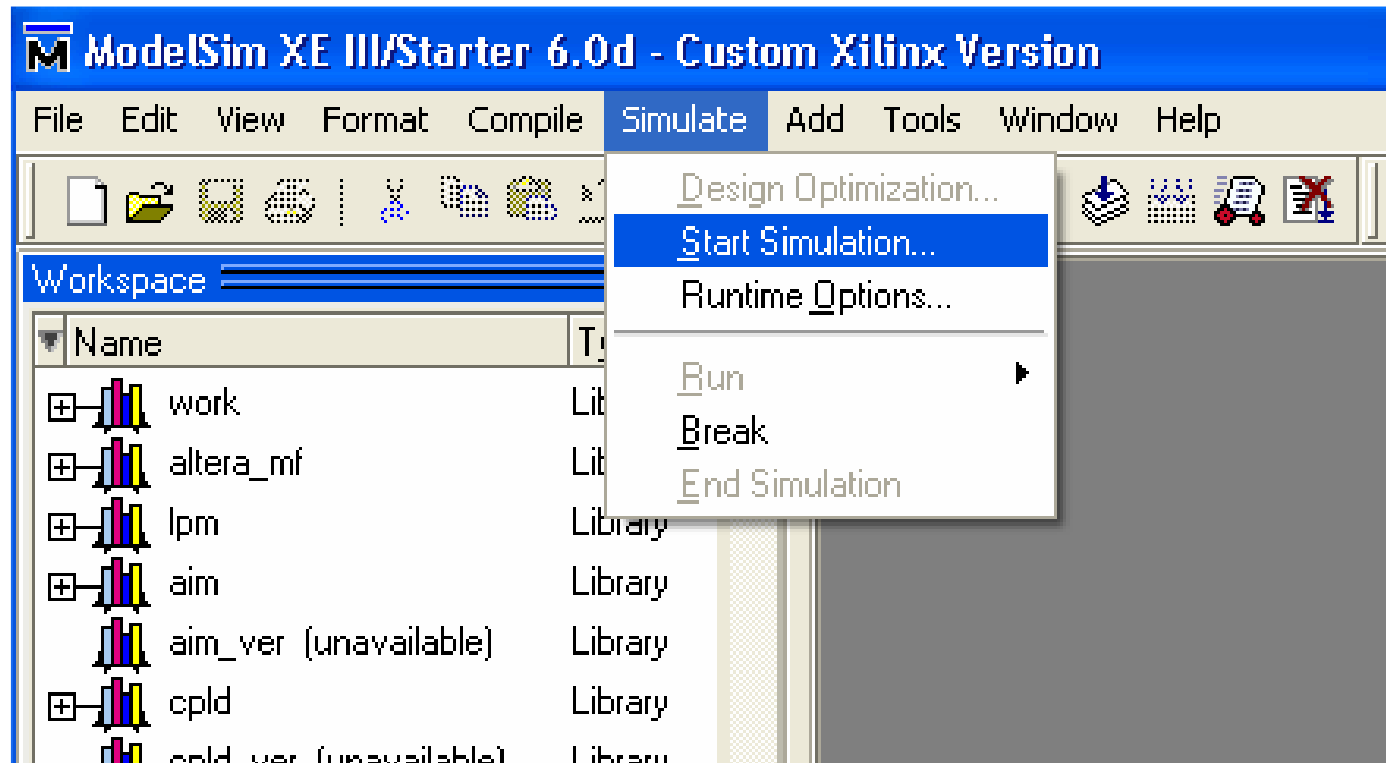
- Check that the compilation was successful and no warnings or errors were reported in the transcript window.



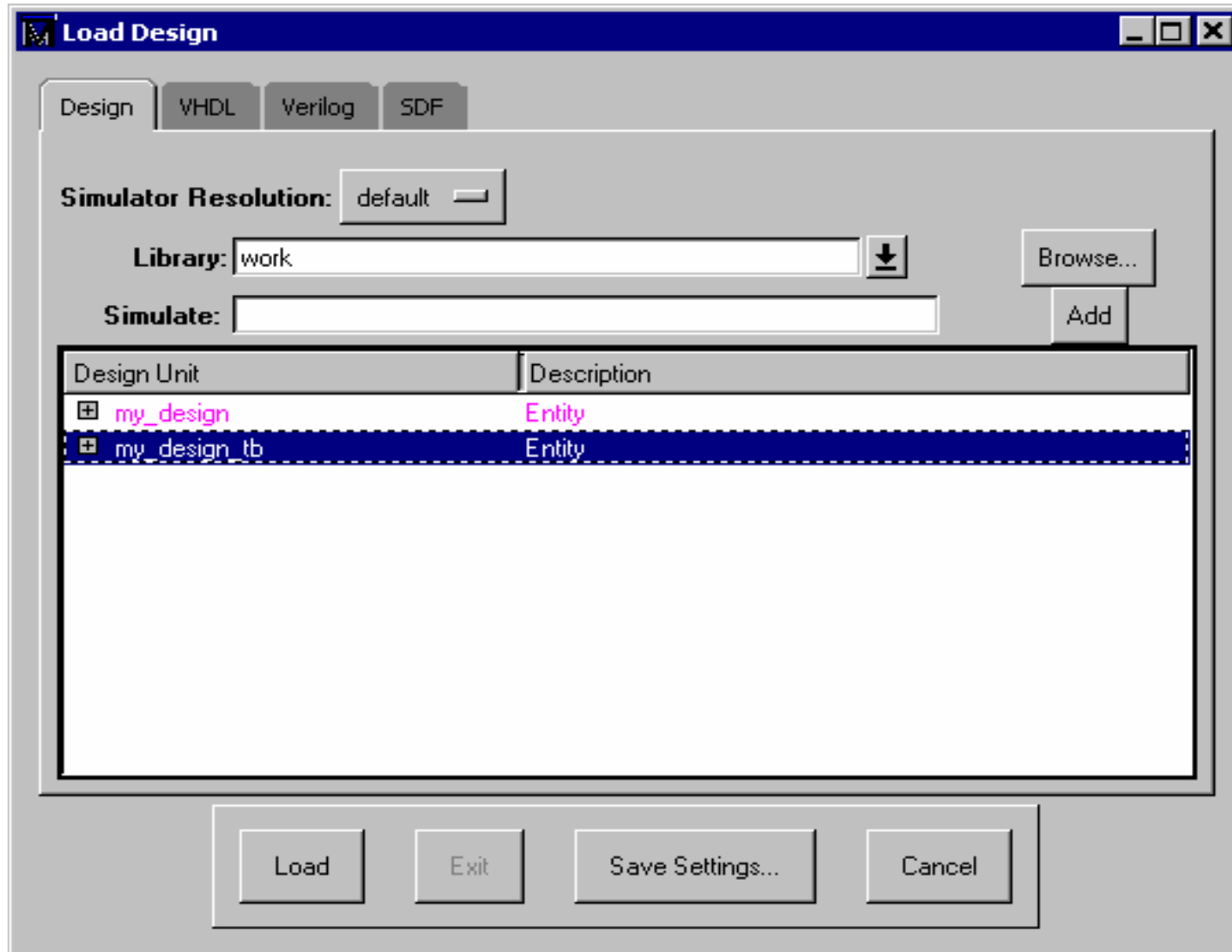
```
ModelSim SE/EE PLUS 5.4b
File Edit Design View Run Macro Options Window Help
exec vlib work
exec vmap work work
# Modifying modelsim.ini
vcom -reportprogress 300 -work work {C:/vhdl/my_design.vhd}
# Model Technology ModelSim SE/EE vcom 5.4b Compiler 2000.06 Jun 8 2000
# -- Loading package standard
# -- Loading package std_logic_1164
# -- Compiling entity my_design
# -- Compiling architecture arc_my_design of my_design
vcom -reportprogress 300 -work work {C:/vhdl/my_design_tb.vhd}
# Model Technology ModelSim SE/EE vcom 5.4b Compiler 2000.06 Jun 8 2000
# -- Loading package standard
# -- Loading package std_logic_1164
# -- Compiling entity my_design_tb
# -- Compiling architecture htwttestbench of my_design_tb
# -- Loading entity my_design

ModelSim> |
<No Design Loaded>
```

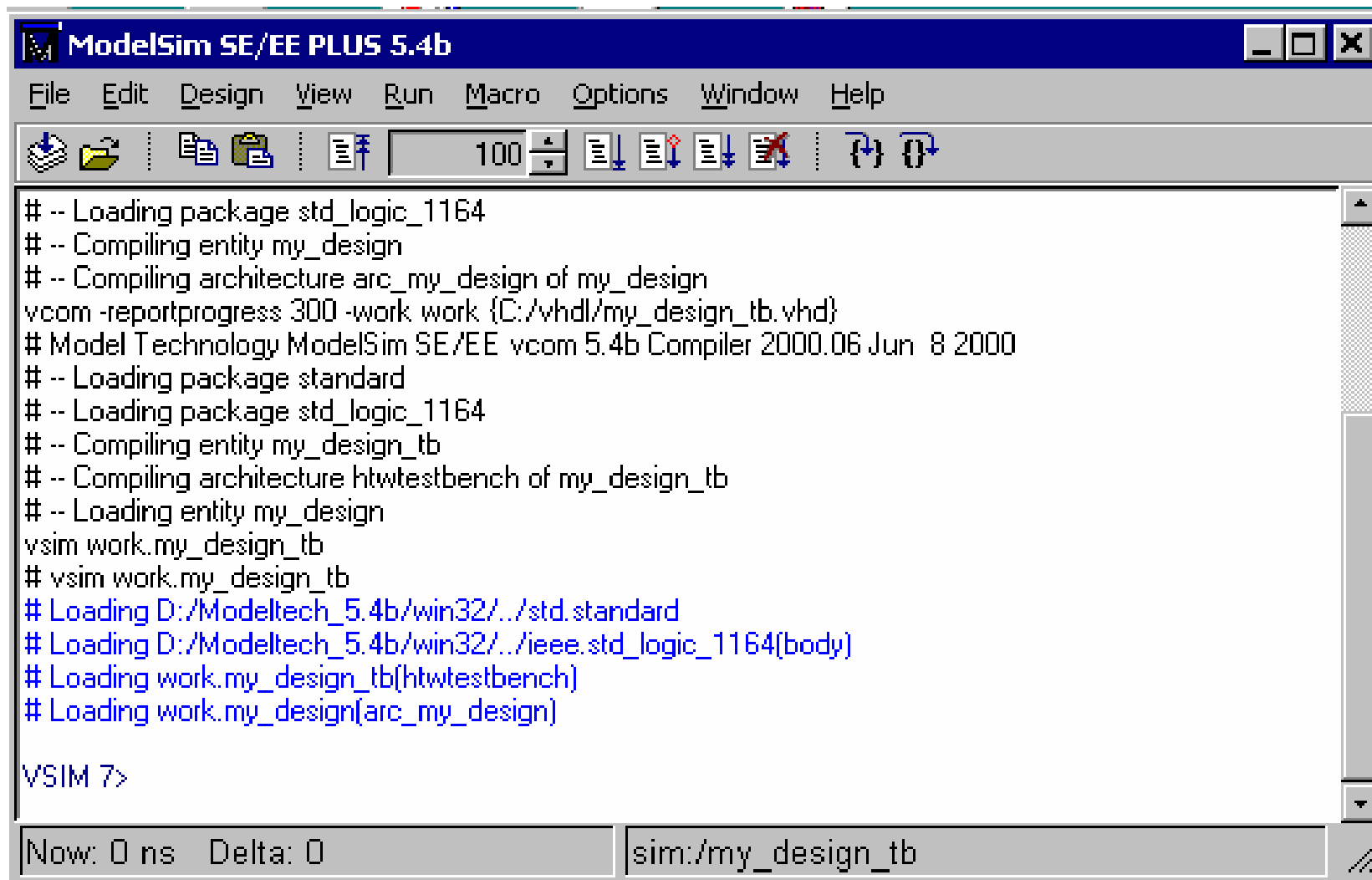
- The next step is to load the test bench to the simulator. Choose Simulate\Start Simulation...



- Mark the desired test bench and click LOAD...



- Make sure that the loading was successful
(No warnings/errors in transcript window)...



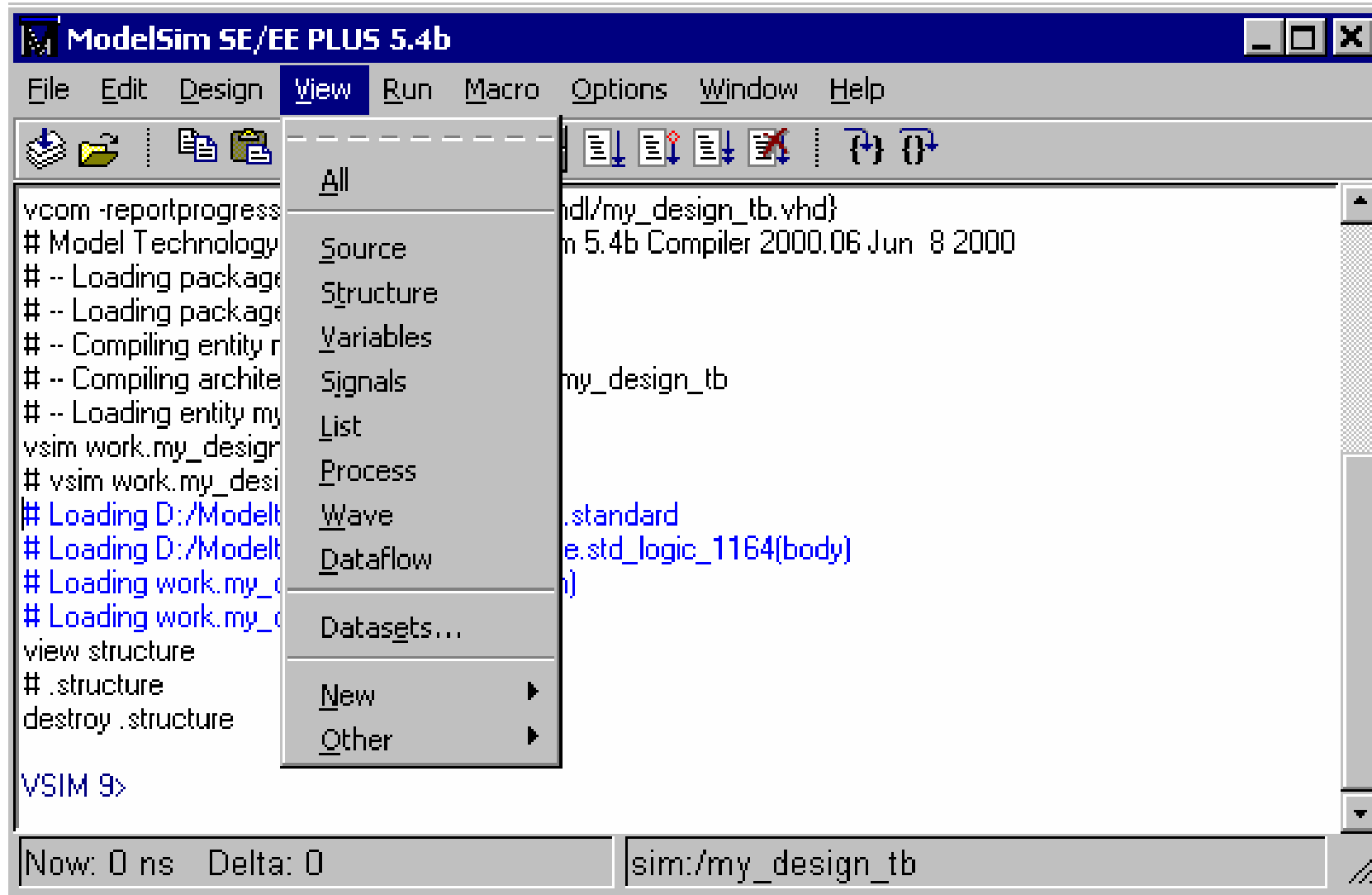
The screenshot shows the ModelSim SE/EE PLUS 5.4b interface. The title bar reads "ModelSim SE/EE PLUS 5.4b". The menu bar includes File, Edit, Design, View, Run, Macro, Options, Window, and Help. The toolbar contains icons for file operations and simulation controls, with a zoom level of 100. The main transcript window displays the following text:

```
# -- Loading package std_logic_1164
# -- Compiling entity my_design
# -- Compiling architecture arc_my_design of my_design
vcom -reportprogress 300 -work work {C:/vhdl/my_design_tb.vhd}
# Model Technology ModelSim SE/EE vcom 5.4b Compiler 2000.06 Jun  8 2000
# -- Loading package standard
# -- Loading package std_logic_1164
# -- Compiling entity my_design_tb
# -- Compiling architecture htwtestbench of my_design_tb
# -- Loading entity my_design
vsim work.my_design_tb
# vsim work.my_design_tb
# Loading D:/Modeltech_5.4b/win32/./std.standard
# Loading D:/Modeltech_5.4b/win32/./ieee.std_logic_1164(body)
# Loading work.my_design_tb(htwtestbench)
# Loading work.my_design(arc_my_design)

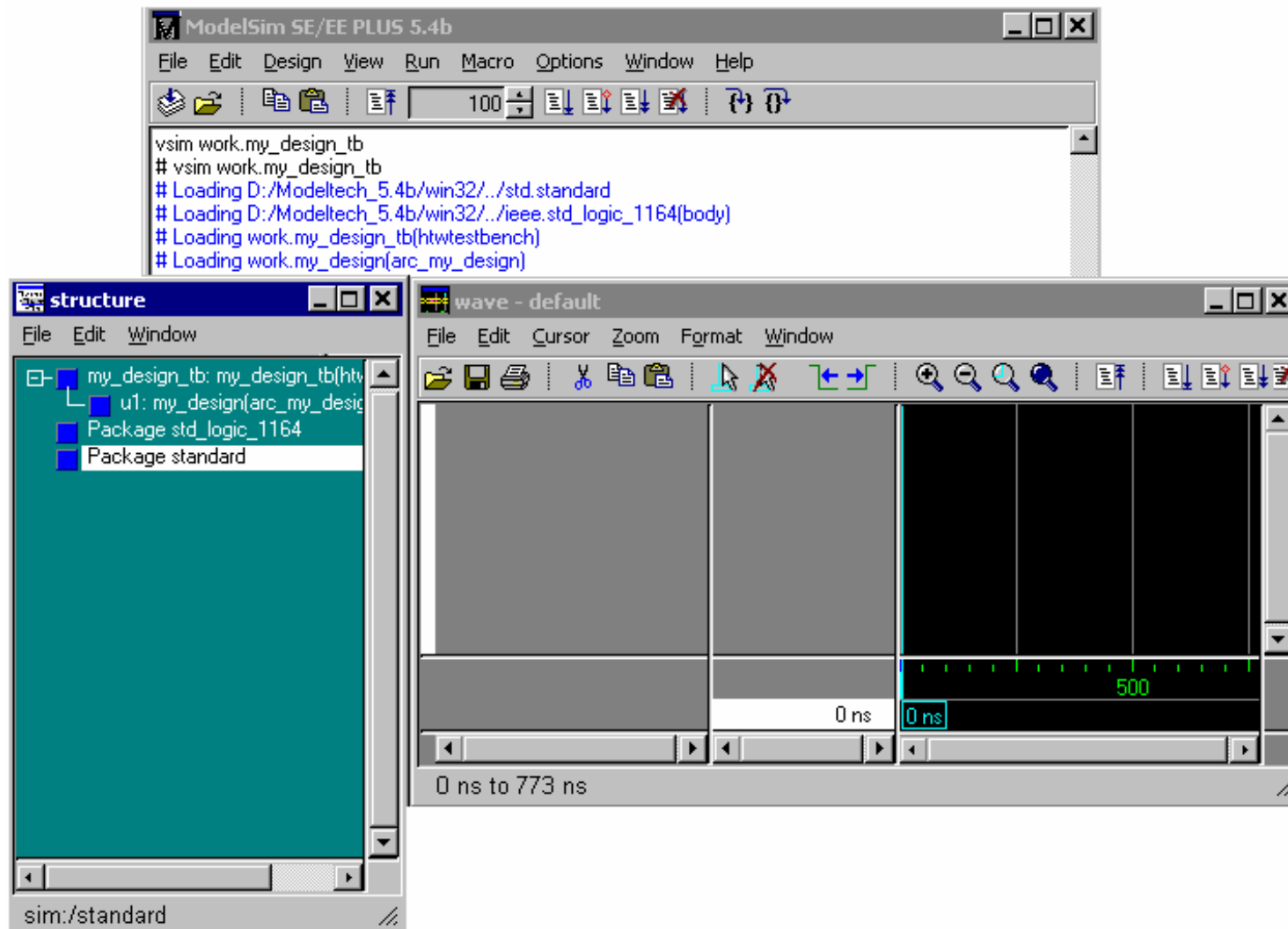
VSIM 7>
```

At the bottom, the status bar shows "Now: 0 ns Delta: 0" and "sim:/my_design_tb".

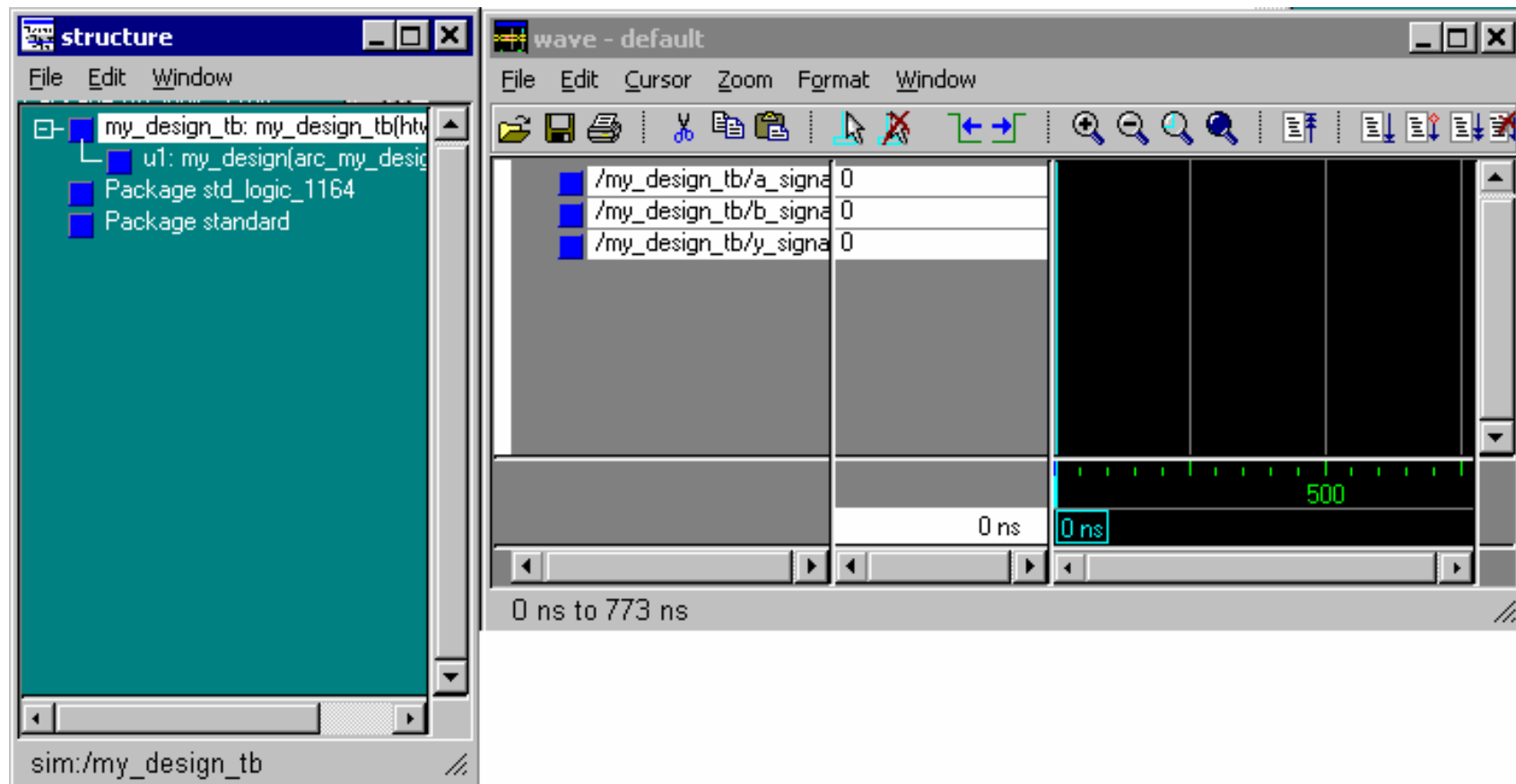
- Click VIEW...



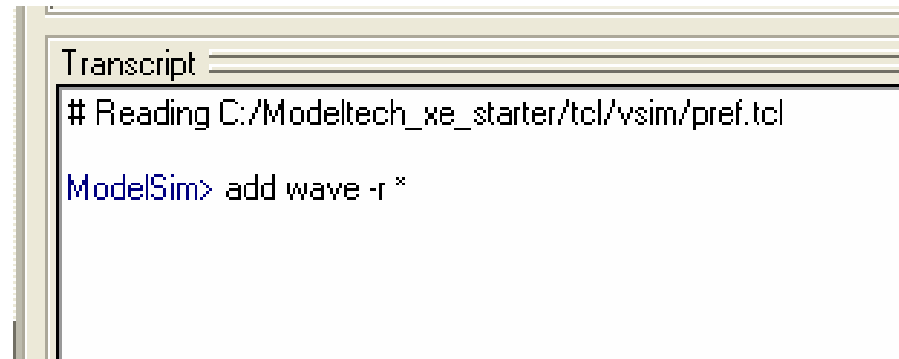
- Open the following windows: Structure, Wave...



- Drag the chosen test bench from the STRUCTURE and drop it in the WAVE window...

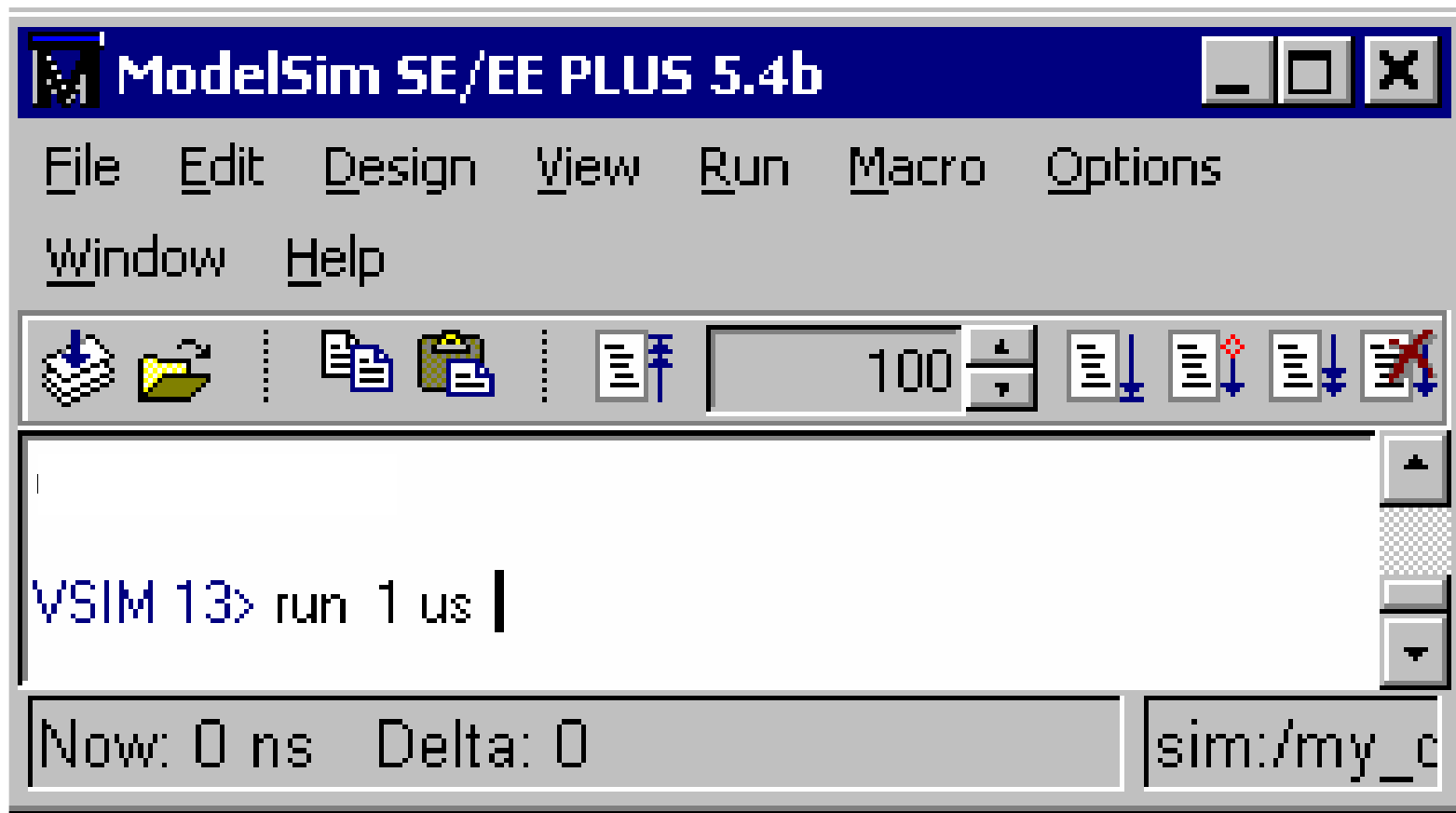


- The another way to insert signals to wave window: Make transcript window active and write in the command line add **wave -r ***. Press Enter...

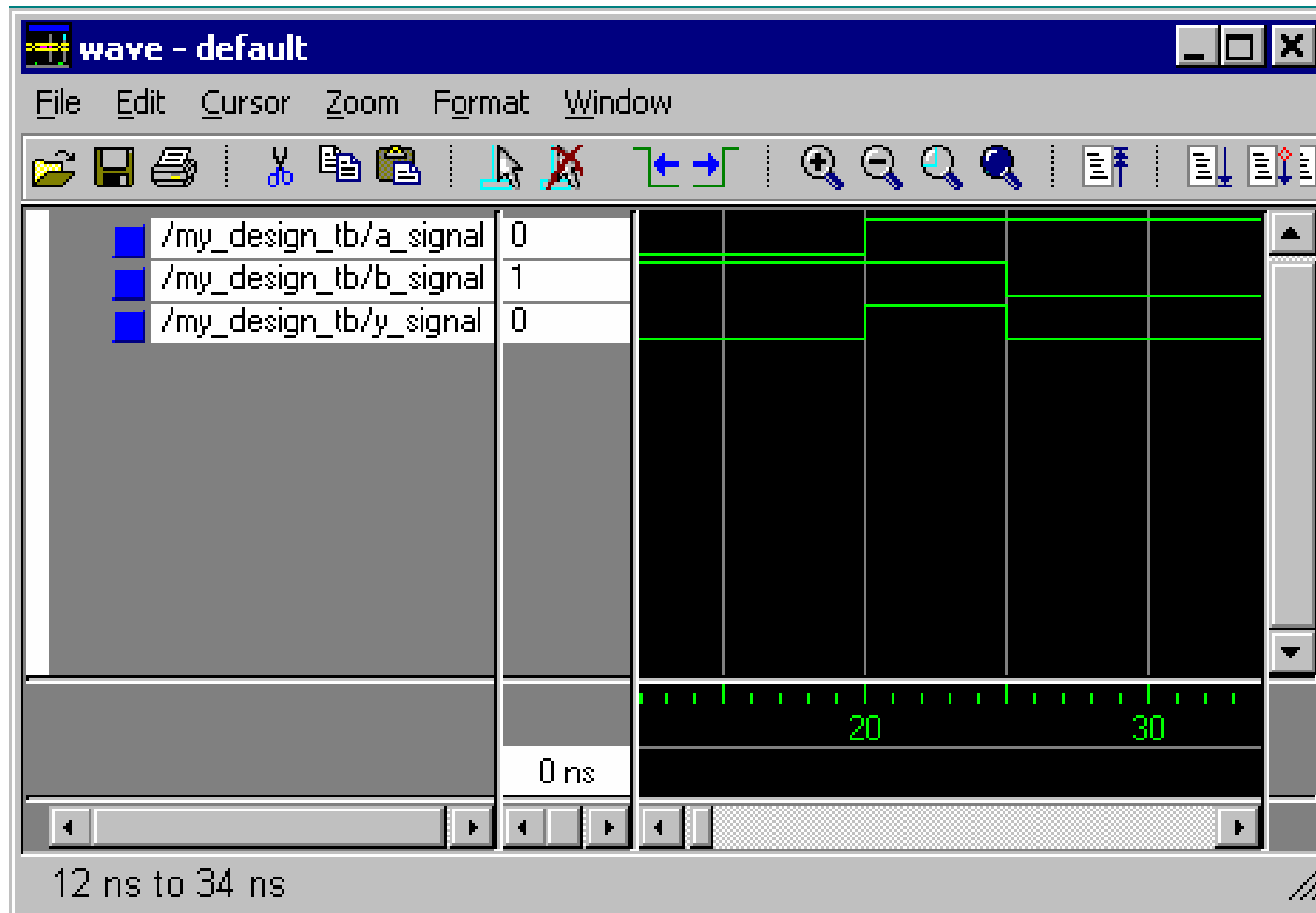


```
Transcript  
# Reading C:/Modeltech_xe_starter/tcl/vsim/pref.tcl  
ModelSim> add wave -r *
```

- Make transcript window active and write in the command line desired simulation time. Press Enter...



- Check the received waveform and verify that your design functions correctly.



Useful commands

- `cd {full_path}` - change directory
- `pwd` -print name of current/working directory
- `vlib {folder name}` – create folder
- `vmap {physical_folder work }` – mapping to virtual folder “work”
- `vcom -93 –quiet –work work {full_path/ file name.vhd}` – compile the chosen file to work
- `vsim –t {units} work.test_bench_entity_name`
 - load simulation
- `add wave –r *` - add all wave (recursive search) to simulation window
- `run t units` – run simulation for t time units
- `restart –f` - reload simulation
- `quit –sim` – end of current simulation
- `quit –f` - kill process (modelsim)
- `.main clear` – clear the transcript window
- `notepad` – open the Modelsim build-in editor
- `alias new_name original_name` – allows to rename existing command
 - For example : `alias cls .main clear`