

## Verilog Coding Guidelines \*

### **Guideline 1:**

When modeling **sequential** logic, use **non-blocking** assignments.

### **Guideline 2:**

When modeling **latches**, use **non-blocking** assignments.

### **Guideline 3:**

When modeling **combinational** logic with an *always* block, use **blocking** assignments.

### **Guideline 4:**

When modeling **both sequential and combinational** logic within the same *always* block, use **non-blocking** assignments.

### **Guideline 5:**

**Do not mix** blocking and non-blocking assignments in the **same always block**.

### **Guideline 6:**

**Do not make** assignments to the **same variable** from more than one *always* block.

### **Guideline 7:**

**Use \$strobe** to display values that have been assigned using **non-blocking** assignments.

### **Guideline 8:**

Do not make assignments using *#0* delays.

\*Suggested by Cliff Cummings "Non-blocking Assignments in Verilog Synthesis, Coding Styles That Kill!" SNUG 2000